

WHAT IS CLAIMED IS:

- 1 1. A multi chip module package structure with low cost and high
2 reliability, comprising:
 - 3 a substrate;
 - 4 a plurality of chip package bodies;
 - 5 a plurality of electrical connect points, electrically connecting the chip
6 package bodies and the substrate;
 - 7 a plurality of electrical connect pins; and
 - 8 a package material, enclosing the substrate, connect points, and chip
9 package body.
- 1 2. The structure as claimed in claim 1, wherein said chip package body is a
2 chip-scale package (CSP) or wafer level CSP.
- 1 3. The structure as claimed in claim 1, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.
- 1 4. The structure as claimed in claim 1, wherein at least one of said chip
2 package bodies is a CSP with a flip chip bonding.
- 1 5. The structure as claimed in claim 1, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.
- 1 6. The structure as claimed in claim 1, wherein said chip package bodies
2 pass burn-in test and function test.
- 1 7. The structure as claimed in claim 2, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.
- 1 8. The structure as claimed in claim 2, wherein at least one of said chip

2 package bodies CSP with a flip chip bonding.

1 9. The structure as claimed in claim 2, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.

1 10. The structure as claimed in claim 2, wherein said chip package bodies
2 pass burn-in test and function test.

3 11. The structure as claimed in claim 1, wherein said plurality of electrical
4 connect pins are solder balls.

1 12. The structure as claimed in claim 1, wherein said plurality of electrical
2 connect points are solder balls or gold wires.

1 13. A multi chip module package structure with low cost and high
2 reliability, comprising:

3 a substrate;

4 at least one chip;

5 one or more than one chip package bodies;

6 a plurality of electrical connect points, electrically connecting the chip
7 package bodies and the substrate;

8 a plurality of electrical connect pins; and

9 a package material, enclosing the substrate, connect points, chips, and
10 chip package bodies.

1 14. The structure as claimed in claim 13, wherein said chip is a bare chip.

1 15. The structure as claimed in claim 14, wherein at least one chip is
2 bonded to the substrate by wire bonding or flip chip bonding.

1 16. The structure as claimed in claim 13, wherein said chip package body

2 is a chip-scale package (CSP) or wafer level CSP.

1 17. The structure as claimed in claim 13, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.

1 18. The structure as claimed in claim 13, wherein at least one of said chip
2 package bodies is a CSP with a flip chip bonding.

1 19. The structure as claimed in claim 13, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.

1 20. The structure as claimed in claim 13, wherein said chip package bodies
2 pass burn-in test and function test.

1 21. The structure as claimed in claim 16, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.

1 22. The structure as claimed in claim 16, wherein at least one of said chip
2 package bodies is a CSP with a flip chip bonding.

1 23. The structure as claimed in claim 16, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.

1 24. The structure as claimed in claim 16, wherein said chip package bodies
2 pass burn-in test and function test.

1 25. The structure as claimed in claim 13, wherein said plurality of
2 electrical connect pins are solder balls.

1 26. The structure as claimed in claim 13, wherein said plurality of
2 electrical connect points are solder balls or gold wires.

1 ~~27. A method of packaging multi chip module at low cost and with high~~
2 ~~reliability to form multi chip module package containing a plurality of~~

3 chips bonded to a substrate as a main body, wherein said method is
4 characterized as: using one or more than one chip package body as CSP,
5 which is electrically connected to the substrate to form said main body.

1 28. The method as claimed in claim 27, wherein said main body may form
2 a plurality of electrical connect pins and is enclosed by a package material.

1 29. The method as claimed in claim 28, wherein said plurality of electrical
2 connect pins are solder balls.

1 30. The method as claimed in claim 27, wherein said chip package body is
2 of chip-scale package (CSP) or wafer level CSP.

1 31. The method as claimed in claim 27, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.

1 32. The method as claimed in claim 27, wherein at least one of said chip
2 package bodies is a CSP with a flip chip bonding.

1 33. The method as claimed in claim 27, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.

1 34. The method as claimed in claim 27, wherein said chip package bodies
2 pass burn-in test and function test.

1 35. The method as claimed in claim 30, wherein at least one of said chip
2 package bodies is a CSP with a wire bonding.

1 36. The method as claimed in claim 30, wherein at least one of said chip
2 package bodies is a CSP with a flip chip bonding.

1 37. The method as claimed in claim 30, wherein at least one of said chip
2 package bodies is a CSP with a central pad bonding.

- 1 38. The method as claimed in claim 30, wherein said chip package bodies
2 pass burn-in test and function test.
- 1 39. The method as claimed in claim 27, wherein said chip package body
2 has a height less than 1.00 mm.
- 1 40. The method as claimed in claim 27, wherein said chip package body
2 has a plurality of electrical connect points, which are solder balls or gold
3 wires.
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